

REMARKS

Claims 1-5, 7-10, and 12-16 are now pending in the application. By this paper, Claims 1, 12, and 13 have been amended. The basis for these amendments can be found throughout the specification, claims, and drawings originally filed. No new matter has been added. The preceding amendments and the following remarks are believed to be fully responsive to the outstanding Office Action and are believed to place the application in condition for allowance.

The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 103

Claims 1-5, 7-10 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nishimura et al. (U.S. Pat. No. 6,781,241) in view of Yamamoto (JPO 2001-110979).

Claims 12 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nishimura et al. (U.S. Pat. No. 6,781,241) in view of Yamamoto (JPO 2001-110979).

Claim 13 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Nishimura et al. (U.S. Pat. No. 6,781,241) in view of Yamamoto (JPO 2001-110979).

Claim 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Nishimura et al. (U.S. Pat. No. 6,781,241), Yamamoto (JPO 2001-110979) and Wachtler (U.S. Publication 20030022465).

These rejections are respectfully traversed.

Independent Claim 1 calls for a semiconductor device including a first semiconductor chip having a mounting face and a reverse face formed on an opposite side of the first semiconductor chip from the mounting face. The first semiconductor chip is mounted face down on a first carrier substrate such that the mounting face opposes the first carrier substrate. A second carrier substrate is held above, and spaced apart from, the first semiconductor chip such that a gap is created between the first semiconductor chip and the second carrier substrate, exposing the reverse face of the first semiconductor chip.

Independent Claim 12 calls for an electronic device including a first carrier substrate, a first electronic part mounted on the first carrier substrate, a second carrier substrate, and a second electronic part mounted on the second carrier substrate. Protruding electrodes connect the second carrier substrate to the first carrier substrate such that the second carrier substrate is held above, and spaced apart from, the first electronic part. A gap is created between a top surface of the first electronic part and the carrier substrate, exposing the top surface of the first electronic part. Similarly, independent Claim 13 calls for an electronic apparatus including a first carrier substrate, a first semiconductor chip mounted on the first carrier substrate, a second carrier substrate, and second semiconductor chip mounted on the second carrier substrate. Protruding electrodes connect the second carrier substrate to the first carrier substrate such that the second carrier substrate is held above, and spaced apart from, the first semiconductor chip. A gap is created between a top surface of the first semiconductor chip and the second carrier substrate, exposing the top surface of the first semiconductor chip.

Independent Claim 12 calls for a method of manufacturing a semiconductor device including mounting a first semiconductor chip face down on a first carrier substrate so that the reverse face of the first semiconductor chip is exposed, mounting a second semiconductor chip on a second carrier substrate, and sealing the second semiconductor chip with a sealing resin. The second carrier substrate is held above the first semiconductor chip by protruding electrodes so as to be separated from the first semiconductor chip. Similarly, independent Claim 16 calls for a method of manufacturing an electronic device, including mounting a first electronic part on a first carrier substrate so that the reverse face of the first electronic part is exposed, mounting a second electronic part on a second carrier substrate, and sealing the electronic part with a sealing resin. The second carrier substrate is connected to the first carrier substrate by protruding electrodes such that the second carrier substrate is held above, and separated from, the first electronic part.

Nishimura discloses a stacked-type semiconductor device including a first substrate (1b), a second substrate (1a), a first semiconductor chip (3b), and a second semiconductor chip (3c). See Nishimura at FIG. 8. The second substrate is positioned above the first substrate such that the first semiconductor chip is positioned generally between a top portion of the first substrate and a bottom portion of the second substrate. See Nishimura at FIGS. 8 and 16. While the second substrate is positioned above the first semiconductor chip, the second substrate is not held above, and spaced apart from, the first semiconductor chip as the first semiconductor chip is connected to the second substrate by adhesives (9, 12). See Nishimura at FIGS. 8 and 16.

The Examiner cites Yamamoto as teaching stacked semiconductor chips having a first substrate (20), a second substrate (15), and a first semiconductor chip (19). See Yamamoto at FIG. 1. While the second substrate is held above the first substrate, such that the first semiconductor chip is positioned generally between a top surface of the first substrate and a bottom surface of the second substrate, a conductive spring material (23) connects the first semiconductor chip to the second substrate. See Yamamoto at FIG. 1. In this manner, the second substrate is not held above, and spaced apart from, the first semiconductor chip as the second substrate is connected to the first semiconductor chip by the spring material.

In light of the foregoing, Applicant respectfully submits that the combination of Nishimura and Yamamoto fails to teach connecting a second substrate to a first substrate such that the second substrate is held above, and spaced apart from, a first semiconductor chip mounted on the first substrate. Therefore, Applicant respectfully submits that the combination of Nishimura and Yamamoto fails to teach or suggest providing a gap between a top surface of a first semiconductor chip and a bottom surface of a second substrate such that the top surface of the first semiconductor chip is exposed.

Because Nishimura and Yamamoto do not disclose connecting a second substrate to a first substrate such that the second substrate is held above, and spaced apart from, a first semiconductor chip mounted on the first substrate, and further, because the combination of Nishimura and Yamamoto fails to teach a gap disposed between a top surface of the first semiconductor chip and the second substrate, Applicant's invention is not taught or suggested by the prior art and reconsideration and


withdrawal of the rejection is respectfully requested. In this manner, it is believed that independent Claims 1, 12, 13, 14, and 16, as well as Claims 2-5, 7-10, and 15, respectively dependent therefrom, are in condition for allowance in light of the art of record. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: February 9, 2006

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